



# DATA SHEET

## SPEAKER AMPLIFIER

## TSDP90xx

### DESCRIPTION

The TSDP90xx single-chip integrated speaker amplifier. The high integration of the TSDP90xx enables the smallest PCB footprint with the lowest system BOM count and cost. TSDP90xx provides high quality HD Audio capability. TSDP90XX is a high-performance Class D speaker driver utilizing TSI's DDX technology. Analog Audio input with no need for clock and control-code detection circuitry.

### FEATURES

- **2W/channel Class-D stereo BTL speaker amplifier @ 4 ohms and 5V**
  - **Speaker Protection**
    - Dedicated BTL high pass filter
    - Mono bandpass filter
- 40-pin, 5X5mm QFN RoHS package**

### APPLICATIONS

- **Tablet Computers**
- **Gaming-class Laptops**
- **Portable Gaming Platforms**
- **Digital Audio Streaming / Connected Audio Accessories**
  - Bluetooth™-enabled Docking Stations
  - Wi-Fi (Miracast, Chromecast, AirPlay®)-enabled Docking Stations
  - Lightning-enabled Docking Stations
  - Thunderbolt® I/II/III-enabled Docking Stations / Connectivity Expansion Hubs
  - HDMI™-enabled Docking Stations
  - MHL™-enabled Docking Stations
  - USB 1.1 / 2.0 / 3.0 / 3.1 Gen 1 / 3.1 Gen 2 / USB-C-enabled Docking Stations / Connectivity Expansion Hubs / Tablets / Tablet & Mobile Phone Cases / Portable Projectors
  - Remote Controls / Gaming Controllers with Integrated Audio

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## **1. DESCRIPTION**

### **1.1. Overview**

An integrated BTL stereo amplifier is ideal for driving 4ohm or 8ohm integrated speakers in mobile speaker system.

The TSDP90xx speaker amplifier is offered in a 40-pin QFN Environmental (ROHS) package

### **1.2. Orderable Part Numbers**

TSDP90xx5NDGXyyX	Analog Class-D Speaker Amplifier
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**Table 1. Part Number**

yy = silicon stepping/revision, contact sales for current data.  
Add an "8" to the end for tape and reel delivery.

## 2. DETAILED DESCRIPTION

### 2.1. Port Functionality

- BTL stereo output
- Line In

#### 2.1.1. Filter Description

The band-pass filter is derived from the common biquadratic filter and provides a 12dB/octave roll-off.

The band-pass filter is enabled by default with a cut-off frequencies at 120Hz and 250Hz.

### 2.2. MUTE

The MUTE pin (pin 40) operates as an external amplifier power up signal. The MUTE value is reflected on the MUTE pin; a 1 causes the external amplifier to power up and a 0 causes it to power down. The pin defaults to an open-drain configuration (an external pull-up is recommended.)

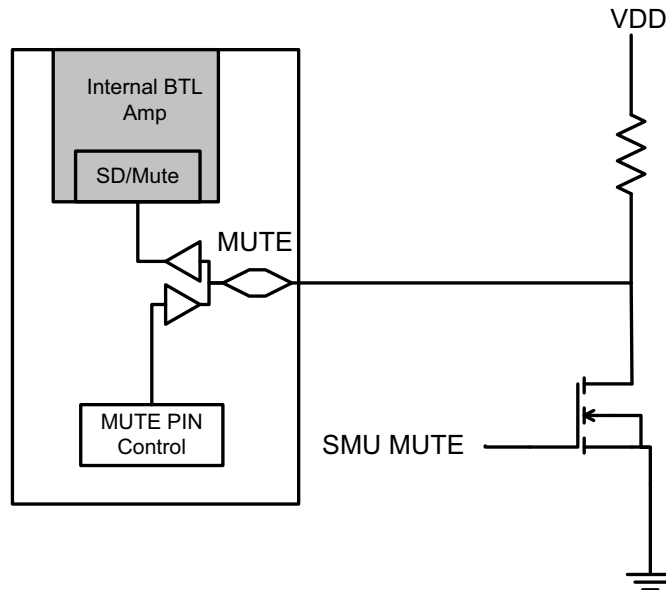


Figure 1. MUTE implementation

## 2.3. BTL Amplifier

An integrated class-D stereo BTL amplifier is provided to directly drive 4 ohm speakers (2W @ 4.75V) or 8 ohm speakers (1W @ 4.75V). No external filter is needed for cable runs of 18" or less. An internal DC blocking filter prevents distortion when the audio source has DC content, and prevents unintentional power consumption when pausing audio playback. The amplifier may be controlled using the MUTE pin (see MUTE section.)

The BTL amplifier includes thermal management circuitry. When the CODEC reaches a temperature of about 140 degrees, the output amplitude of the BTL amp is gradually lowered until the temperature falls below 140. All other functions will remain active if the BTL amplifier is shut down due to die temperature.

## 2.4. BTL Amplifier High-Pass Filter

For mobile applications, speakers are often incapable of reproducing low frequency audio and unable to handle the maximum output power of the BTL amplifier. A high-pass filter is implemented in the BTL output path to reduce the amount of low frequency energy reaching speakers attached to the BTL amplifier. This can prevent speaker failure.

### 2.4.1. Filter Description

The high-pass filter is derived from the common biquadratic filter and provides a 12dB/octave roll-off.

## 2.5. Digital Core Voltage Regulator

The digital core operates from a 1.8V (10%) supply voltage. Many systems require a single 3.3V digital supply, so an integrated regulator is included on die. The regulator uses pin 7, DVDD, as its voltage source. The output of the LDO is connected to pin 1 and the digital core. A 10uF capacitor must be placed on pin 1 for proper load regulation and regulator stability.

The digital core voltage regulator is only dependent on DVDD.

## 2.6. "Playback Path" Port Behavior (Analog I/O)

Line In input is routed to speakers.

### 3. CHARACTERISTICS

#### 3.1. Electrical Specifications

##### 3.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the TSDP90xx. These ratings, which are standard values are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
	PVdd	6 Volts
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 °C to +70 °C -40 °C to +85°C (INDUSTRIAL TEMP, see part number list)
Storage temperature		-55 °C to +125 °C
Soldering temperature		Soldering temperature information for all available in the package section of this datasheet.

Table 2. Electrical Specification: Maximum Ratings

##### 3.1.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supplies	DVDD_Core	1.6	1.8	1.98	V
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T <sub>case</sub>			+90	°C
	T <sub>case</sub> Industrial			+110	°C

Table 3. Recommended Operating Conditions

**ESD:** The TSDP90xx is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the TSDP90xx implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

**3.2. Class-D BTL Amplifier Performance**

Parameter	Min	Typ	Max	Unit
Output Power (BTL 4 ohm, 5V, <1% THD+N)	2			W
Output Power (BTL 4 ohm, 5V, <10% THD+N)		3		W
Amplifier Efficiency $\eta$ (4 $\Omega$ , 5V, 2W)		86		%
THD+N (BTL 4 $\Omega$ , 5V, FS)			1	%
THD+N (BTL 4 $\Omega$ , 5V, -3dBFS)		0.3		%
Frequency Response	20	-	20K	Hz
PWM frequency		352.8		KHz
Output voltage noise (4 $\Omega$ , 5V)		65		$\mu$ V
Idle current		3.6		mA
Shutdown current		.2		mA

**Table 4. Class-D BTL Amplifier Performance**

4. FUNCTIONAL BLOCK DIAGRAM

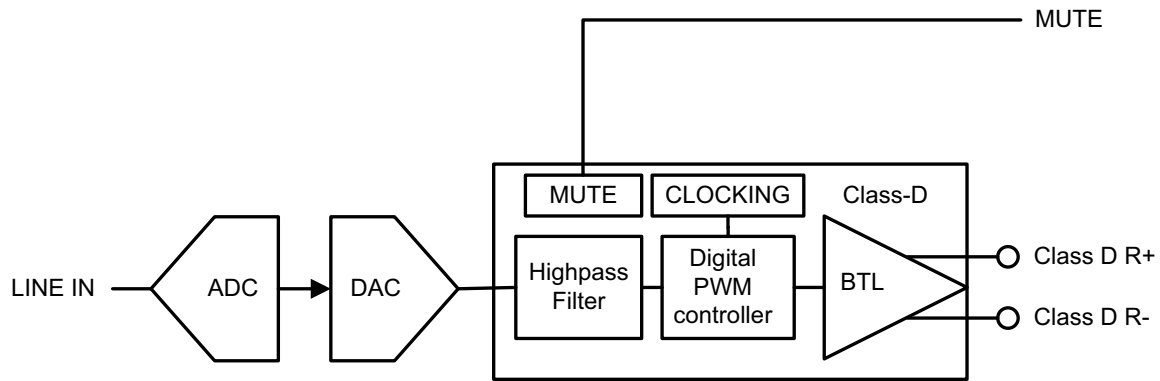


Figure 2. Functional Block Diagram



5. PINOUT AND PACKAGING

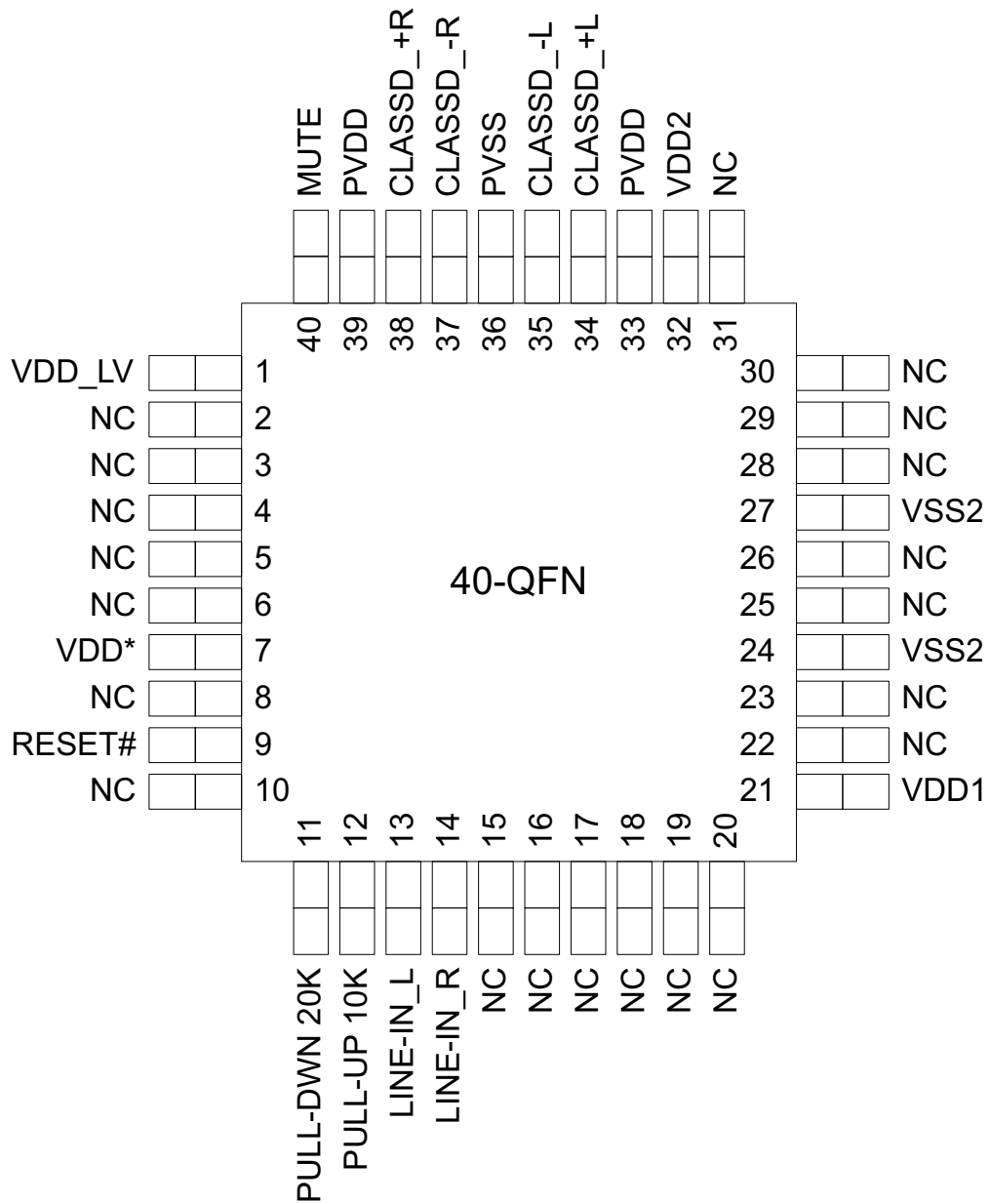


Figure 3. 40QFN Pin Assignment

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**5.0.1. 40QFN Pin Table**

Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	40 pin location
VDD_LV	1.8V Digital Core Regulator Filter Cap	O(Digital)	None	1
VDD	Digital Vdd= 3.3V	I(Digital)	None	7
RESET#	HD Audio Reset	I(Digital)	None	9
PULL-DOWN 20K	Configuration	I(Analog)	None	11
PULL-UP 10K	Jack insertion detection Port F, DMIC0	I(Analog)	None	12
LINE-IN_L	Left input	I/O(Analog)	None	13
LINE-IN_R	Right input	I/O(Analog)	None	14
VDD1	Analog Vdd=5.0V or 3.3V	I(Analog)	None	21
VSS2	Analog Ground	I(Analog)	None	24,27
V-	Negative analog supply	O(Analog)	None	28
CAP-	Charge pump cap -	O(Analog)	None	29
CAP+	Charge pump cap +	O(Analog)	None	30
VREG	Linear Regulator Output (2.5V) filter cap	O(Analog)	None	31
VDD2	Analog Supply for VREG	I(Analog)	None	32
PVDD	Analog Supply for Class-D amp	I(Analog)	None	33
CLASSD_+L	BTL amp Left +	O(Analog)	None	34
CLASSD_-L	BTL amp Left -	O(Analog)	None	35
PVSS	Analog Ground	I(Analog)	None	36
CLASSD_-R	BTL amp Right -	O(Analog)	None	37
CLASSD_+R	BTL amp Right +	O(Analog)	None	38
PVDD	Analog Supply for Class-D amp	I(Analog)	None	39
MUTE	MUTE	I/O (Digital)	60K Pull-up	40
NC	No connect	N?A	None	2,3,4,5, 6,8,10, 15,16, 17,18, 19,20, 22, 23, 25, 26, 28, 29, 30, 31,

**Table 5. 40QFN Pin Description**

5.0.2. 40QFN Package Outline and Package Dimensions

40QFN Package Outline and Package Dimensions

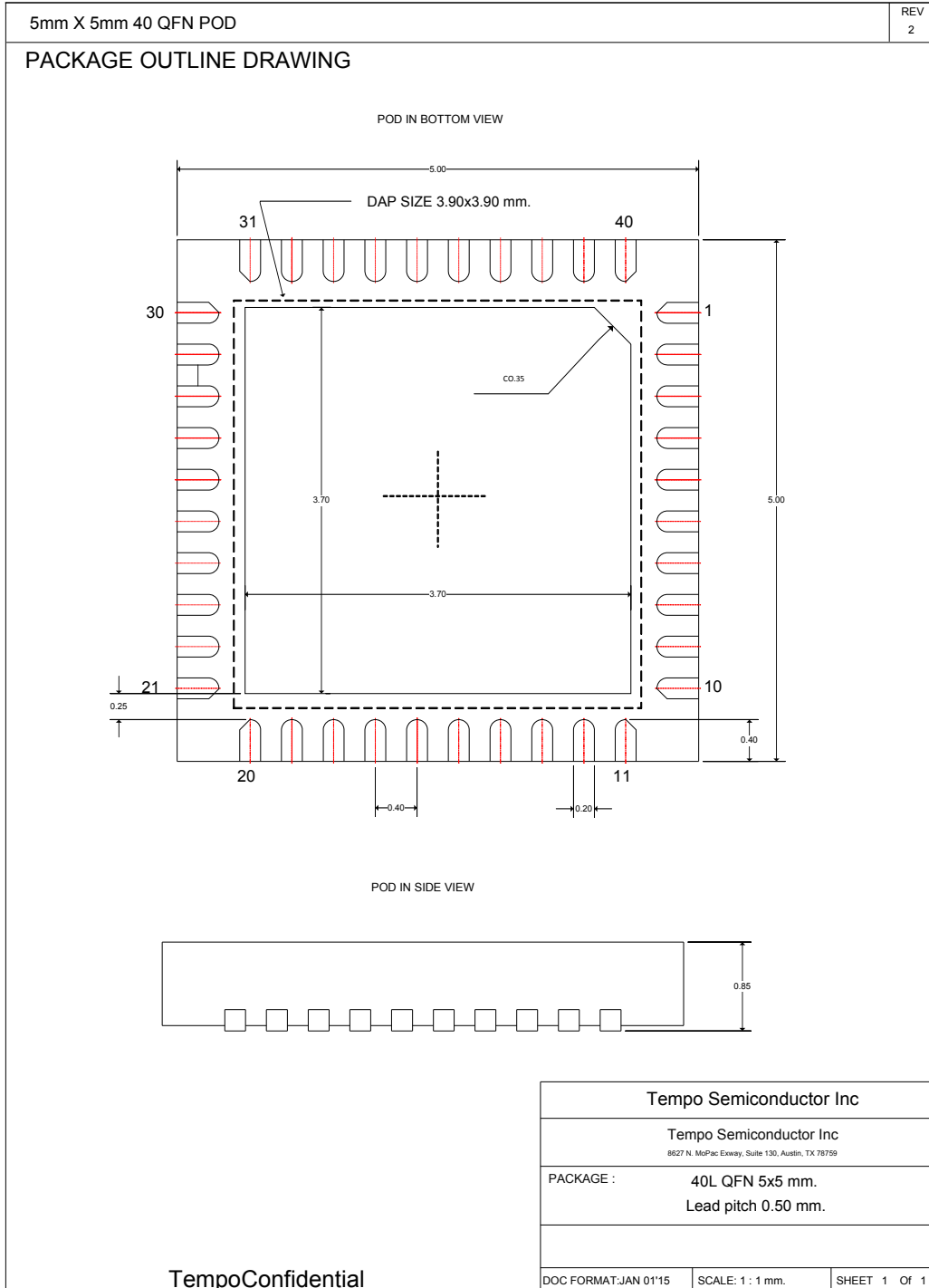


Figure 4. 40QFN Package Diagram

### 5.1. Standard Reflow Profile Data

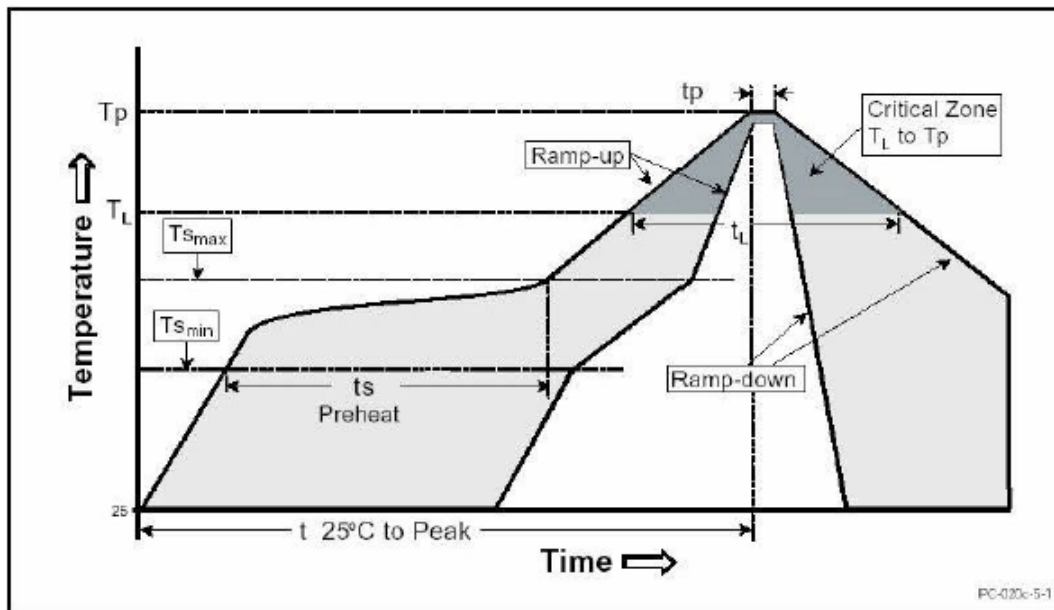
Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

**FROM:** IPC / JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices” ([www.jedec.org/download](http://www.jedec.org/download)).

Profile Feature	Pb Free Assembly
Average Ramp-Up Rate ( $T_{s_{max}} - T_p$ )	3 °C / second max
Preheat: Temperature Min ( $T_{s_{min}}$ ) Temperature Max ( $T_{s_{max}}$ ) Time ( $t_{s_{min}} - t_{s_{max}}$ )	150 °C 200 °C 60 - 180 seconds
Time maintained above: Temperature ( $T_L$ ) Time ( $t_L$ )	217 °C 60 - 150 seconds
Peak / Classification Temperature ( $T_p$ )	See “Package Classification Reflow Temperatures”
Time within 5 °C of actual Peak Temperature ( $t_p$ )	20 - 40 seconds
Ramp-Down rate	6 °C / second max
Time 25 °C to Peak Temperature	8 minutes max

Note: All temperatures refer to topside of the package, measured on the package body surface.

**Table 6. Standard Reflow Profile**



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**6. DOCUMENT REVISION HISTORY**

Revision	Date	Description of Change
0.5	January 2017	Initial release



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