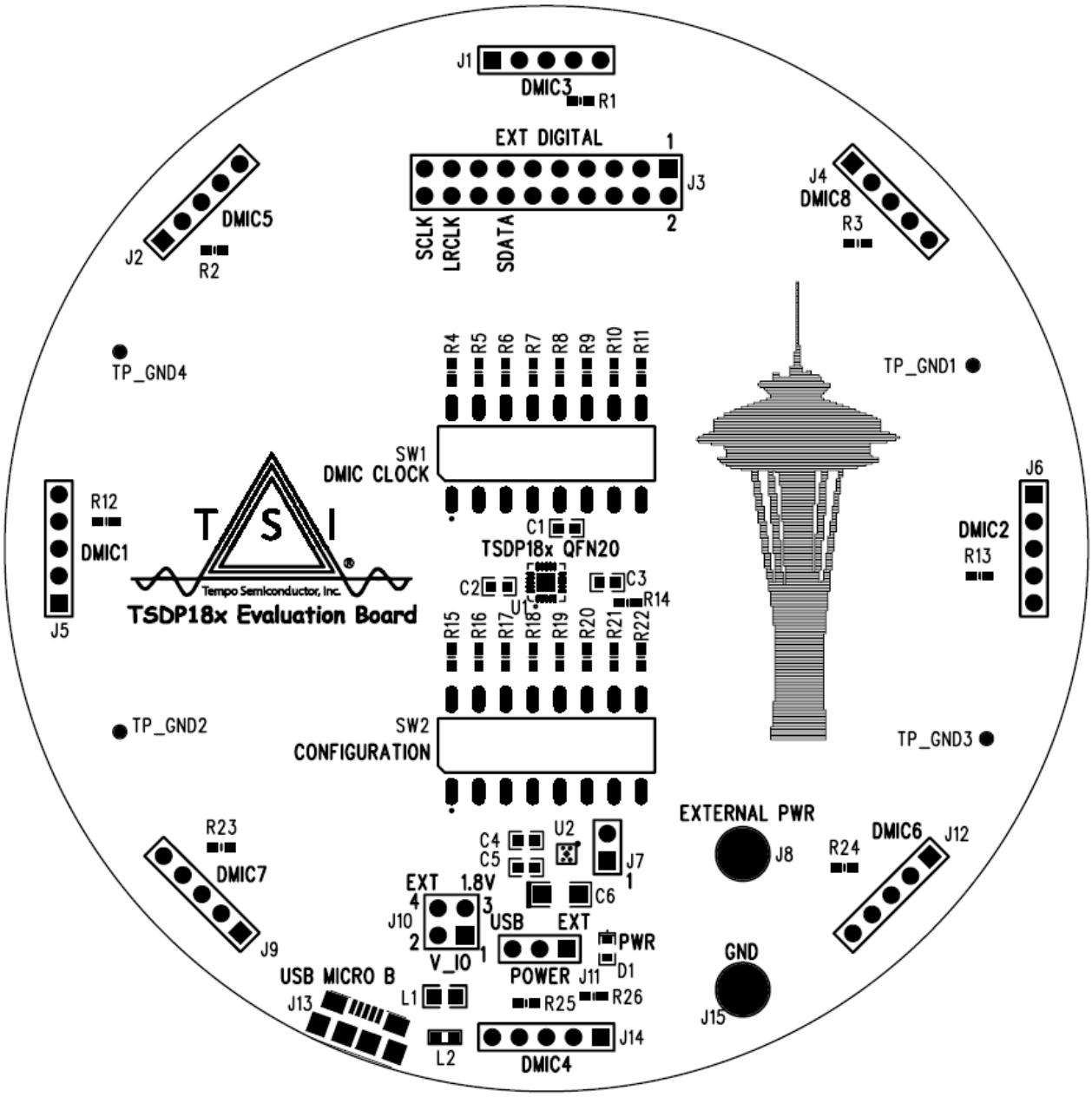
Tempo Semiconductor, Inc.

TSDP18x Evaluation Board User Guide

Rev 0.2 (June 28, 2019)

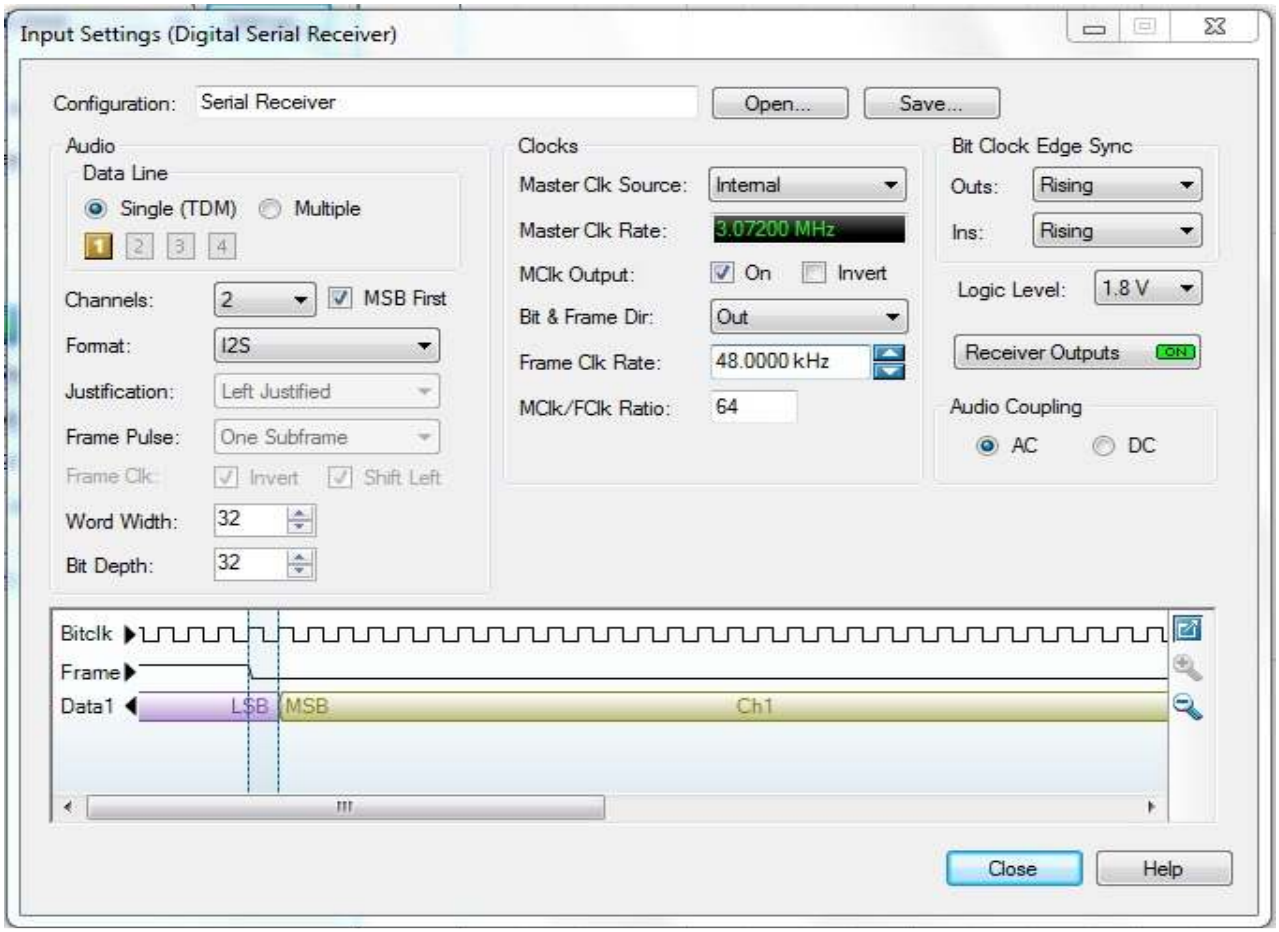

J1
DMIC3
R1
EXT DIGITAL
1
J3
2
SCLK
LRCLK
SDATA
J2
DMIC5
R2
J4
DMIC8
R3
TP_GND4
TP_GND1
R4
R5
R6
R7
R8
R9
R10
R11
SW1
DMIC CLOCK
J6
R12
DMIC1
C1
TSDP18x QFN20
DMIC2
R13
C2
C3
R14
U1
R15
R16
R17
R18
R19
R20
R21
R22
J5
TSDP18x Evaluation Board
TP_GND2
SW2
CONFIGURATION
TP_GND3
EXTERNAL PWR
R23
C4
C5
U2
J7
1
DMIC6
J12
DMIC7
J8
R24
EXT
1.8V
4
3
C6
J10
2
1
USB
EXT
PWR
V_IO
POWER
J11
D1
GND
J9
USB MICRO B
L1
R25
R26
J13
J15
L2
J14
DMIC4

TSDP18x Supported Modes

	Valid PCM Word Slots in TDM Mode SCLK to LRCLK Ratio								
Word Length	**512**	**384**	**256**	**192**	**128**	**96**	**64**	**48**	**32**
32	**8**	**8**	**8**	**6**	**4**	**3**	**2**	**N/A**	**N/A**
24	**8**	**8**	**8**	**8**	**5***	**4**	**2***	**2**	**N/A**
16	**8**	**8**	**8**	**8**	**8**	**6**	**4**	**3**	**2**

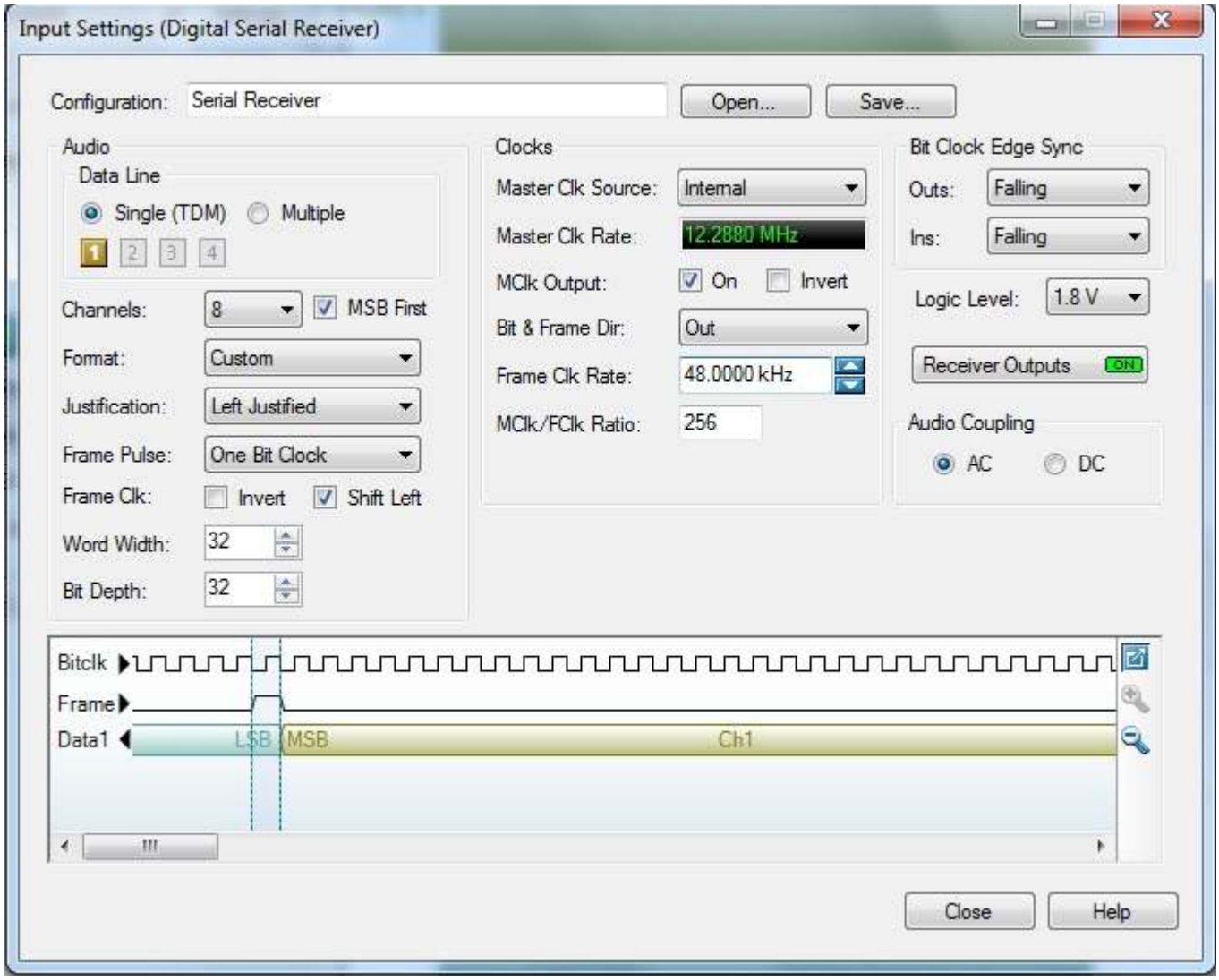
TDM Mode PCM Word Slot Availability based on SCLK to LRCLK Ratio and Word Length

I2S Configuration



This figure shows an example of a typical timing configuration required to support I2S modes. Please note the SCLK and LRCLK relationship, and edge directions.

TDM Configuration



This figure shows an example of a typical timing configuration required to support TDM modes. Please note the SCLK and LRCLK relationship, and edge directions.

Power Connections

The TSDP18x evaluation board can be powered externally in several ways. The part itself needs two voltages, 1.8V for its main supply, and V_IO which must match the signaling voltage and the configuration input signals, and can be either 1.8V or 3.3V.

There is a 1.8V LDO regulator (U2) on the board that can provide 1.8V and it is supplied from either the USB Micro B connector or the External Pwr connection. The jumper at J11 determines which of these inputs provide the source voltage to the LDO. A green LED will indicate that power is being supplied to the LDO. The jumper at J7 must be installed to provide the 1.8V output from the LDO to the TSDP18x itself.

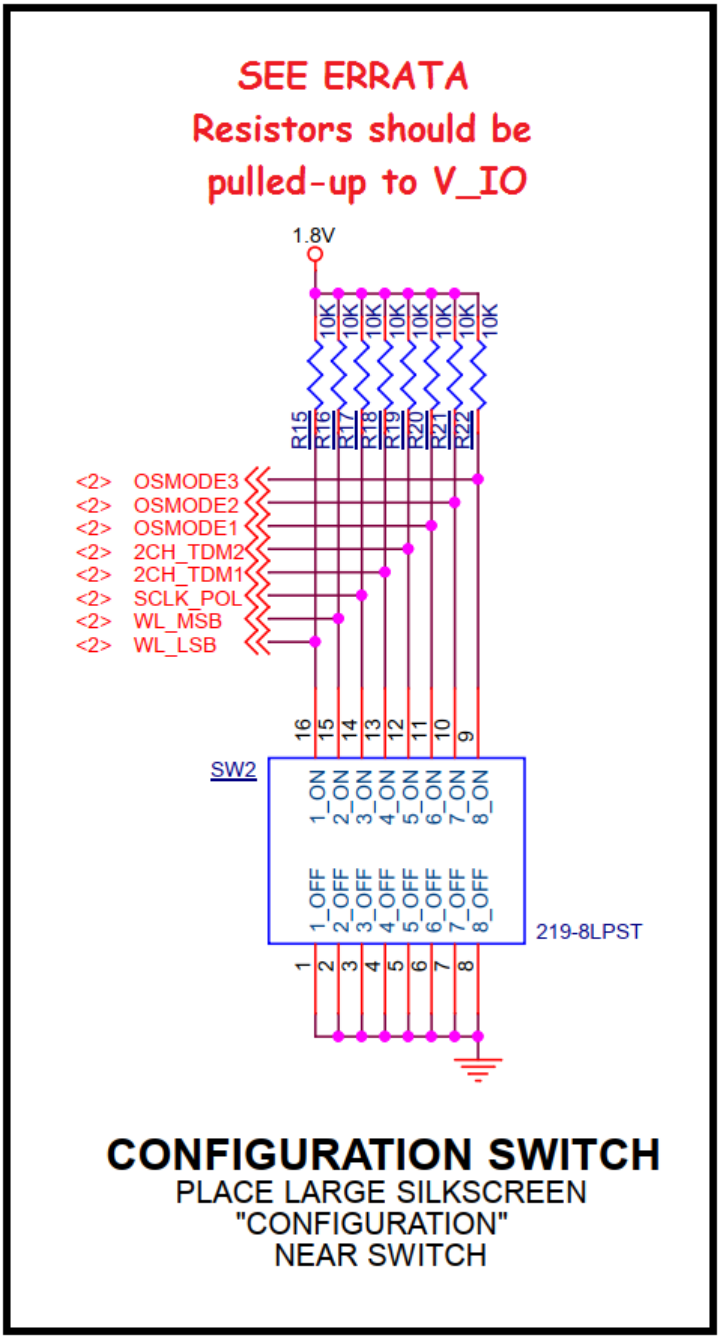
External power can be provided from either the bench supply connectors, J8 and J15, or from the External Digital header, pins 1 and 3. They should be between 2.5V and 5V.

V_IO can be provided from the 1.8V regulator or from an external source. Jumpering 1/3 on connector J10 will use the 1.8V LDO and 2/4 will use an external I/O voltage supplied from the External Digital header, J3 pins 7 and 9.

There are 4 GND test points located at the edges of the board.

SW2 - Configuration Switch

When "ON" this switch will provide a logical low ("0") or GND to the input signal. When "OFF" it will provide a logical high ("1") or V_IO pull-up voltage to the input signal.



	2CH_TDM1	2CH_TDM2
I2S Mode 0, 1 Channel Output Mode, Double-Edged Clocking on PDM Sources	0	0
I2S Mode 1, 2 Channel Output Mode, Single-Edged Clocking on PDM Sources	0	1
Left-Justified, 2 Channel Output Mode, Double-Edged Clocking on PDM Source	1	0
TDM, up to 8 Channel Output Mode, Double-Edged Clocking on PDM Source	1	1

Configuring the PCM Output Format using the 2CH_TDM1 and 2CH_TDM2 Pins

	WL_MSB	WL_LSB
PCM Word Length = 32-bits	0	0
PCM Word Length = 24-bits	0	1
Reserved	1	0
PCM Word Length = 16-bits	1	1

PCM Word Length Configuration using WL_MSB and WL_LSB Pins

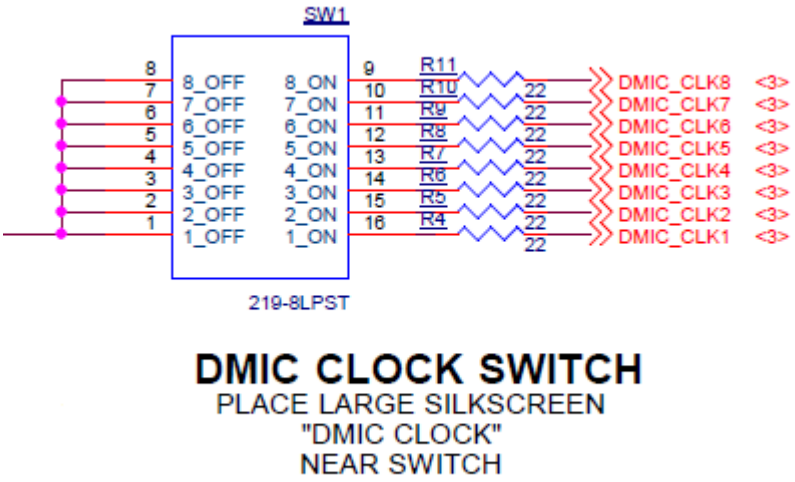
OS_ MODE3	OS_ MODE2	OS_ MODE1	Oversample Rate	Bandwidth at -1dB (Normalized)	Typical Fs Range (kHz)	Valid SCLK / LRCLK Ratios for Corresponding OS_MODE Pin Selection
0	0	0	N/A	N/A	N/A	Reserved
0	0	1	N/A	N/A	N/A	Reserved
0	1	0	8	0.1189	256 to 384	32, 48, 64, 96, 128
0	1	1	16	0.2268	128 to 192	32, 48, 64, 96, 128, 192, 256
1	0	0	32	0.4536	64 to 96	32, 64, 96, 128, 192, 256, 384, 512
1	0	1	48	0.4536	48 to 64	48, 96
1	0	1	64	0.4536	32 to 48	64, 128, 192, 256, 384, 512
1	1	0	96	0.4536	24 to 32	96, 192
1	1	0	128	0.4536	16 to 24	128, 256, 384, 512
1	1	1	192	0.4536	8 to 16	192, 384
1	1	1	256	0.4536	8 to 12	256, 512

Configuring the Oversampling Mode using OS_MODE3, OS_MODE2, OS_MODE1 Pins

SW1 - DMIC Clock Switch

This switch connects the single PDM clock output from the part to each of the eight DMIC connectors. When the switch is set to "ON" the connection is made from pin U1.14 to each of the DMIC connector clock pins, Jx.pin2.

Note: due to the different microphone array options, this node has the potential of variable loading and signal reflections that may produce non-monotonic clock edges or violate timing requirements at the DMIC connectors. For any testing or DMIC connections, the signal integrity must be validated at all destinations. This may involve replacing the series termination resistors, or modifying the connections to the DMIC connectors themselves to make sure that the PDM clock output arrives with the correct setup and hold timings for testing or for the microphone array being evaluated.



J3 - External Digital Header

This header provides the digital interface to the TSDP18x. There are connections for the signals as well as power.

Pin 20 - input for SCLK

Pin 18 - input for LRCLK (frame clock)

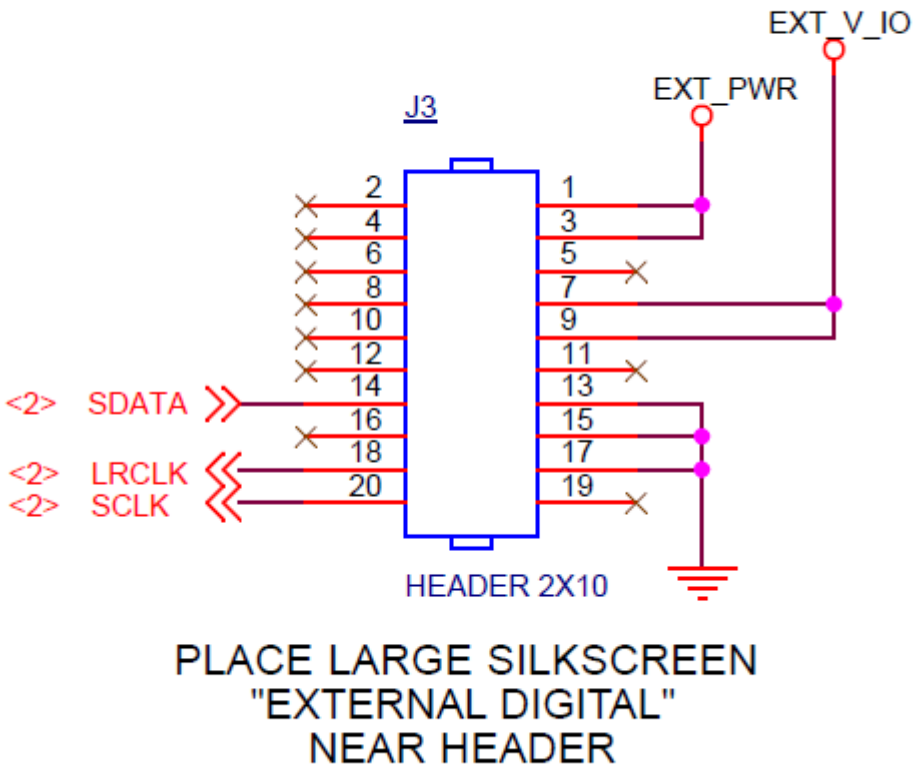
Pin 14 - output of SDATA

Pins 1/3 - external power supply connection

Pins 7/9 - external V_IO supply conneciton

Pins 13/15/17 - GND

Other pins - unused



DMIC Connectors – (J5/J6)/ (J1/J14) / (J2/J12) / (J9/J4)

There are 8 DMIC connectors available for connecting the various array options. They are paired, and pin 3 on each of the connectors will be strapped either to V_IO or GND to select the rising/falling PDM clock edge.

DMIC1/DMIC2 – Use the base pair for I2S, other stereo, and all other array configurations.

DMIC3/DMIC4 – Add pair for quad array configurations.

DMIC5/DMIC6 – Add pair for hex array configurations.

DMIC7/DMIC8 – Add pair for octal array configurations.

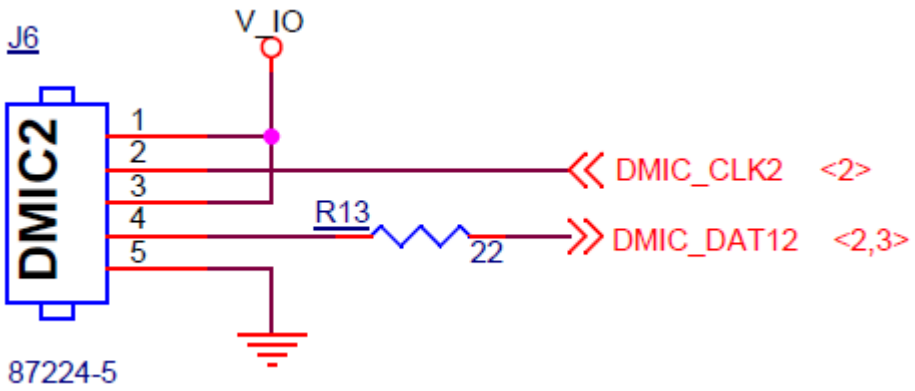
Pin 1 – V_IO power

Pin 2 – PDM Clock

Pin 3 – Select PCM clock edge for data

Pin 4 – PDM Data (paired with other channel DMIC connector)

Pin 5 - GND



Example DMIC Connector Signal Connections

Errata (28Jun19):

- The DMIC5 connector had its clock and data connections incorrectly swapped in the schematic. A rework is required to swap the connections between pins 2 and 4, to match the orientation of the other DMIC connectors.

- The configuration switch resistors are pulled-up to the wrong voltage supply. They should have been pulled-up to V_IO instead of 1.8V. As the 1.8V supply is still above V_IO / 2 even when 3.3V is used for the V_IO voltage, no board rework is required, and all testing to date indicates that the configuration will be set correctly even when using 1.8V as the pull-up voltage with 3.3V V_IO. Customers using the evaluation board as a reference for their own designs should make note of this, especially if they choose to use 3.3V for the V_IO voltage.